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Analog Capacitance ROM with IGFET Bucket-Brigade Shift Register

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Abstract—A new type of monolithic analog read-only memory (AROM) is described. It consists of a memory element and associated on-chip readout circuitry. The memory can be used for storing sample values of time-varying analog signals. The memory element is a matrix of MOS capacitors, preprogrammed in size by a special mask. The readout element is a bucket-brigade (BB) shift register with parallel input and serial output. A test circuit that permits investigation of different principles of information transfer from capacitance matrix to shift register has been developed.

I. Introduction

During the recent years a number of charge-transfer devices have been developed [1]-[3], and some interesting applications as analog delay lines, image sensors, and monolithic transversal filters have emerged from these new devices [1], [4]. In this paper we describe a special kind of analog read-only memory (AROM) which utilizes a bucket-brigade device (BBD) [1] as the readout element.

The basic principle of the AROM is illustrated in Fig. 1. From a store consisting of a matrix of mask-programmed MOS capacitors a signal of n samples is transferred in parallel to an analog shift register. By clocking the shift register, the signal samples are then read out at the serial output of the register.

In the store, each row of capacitors represents a signal with n samples. Each sample value is represented by the size of a MOS capacitor. The store contains m different signals (m rows in the matrix) each of which can be transferred to the BBD analog shift register independent of the others.

In the BBD information is represented by a signal charge on every second capacitor. The remaining capacitors in the BBD contain a reference charge. The transfer of information from the capacitance matrix to the BBD is therefore a transfer of charge between capacitors. The connection between the capacitors is established by a row of MOS transistors, one for each capacitor. After transfer to the BBD every second capacitor C in the BBD must contain a charge which is a function of the size of the capacitor C_j in the store with which charge exchange has taken place. This result can be obtained either by a transfer of charge from C_j to C or by a charge transfer from C to C_j. The two possibilities will be discussed separately in the next section.

II. Circuit Configuration and Operation

Fig. 2 shows a complete circuit diagram of the test circuit for the AROM. The figure will be referred to in the following explanation of the circuit operation. The circuit offers the possibility of testing different principles of charge transfer between capacitance matrix and BBD.

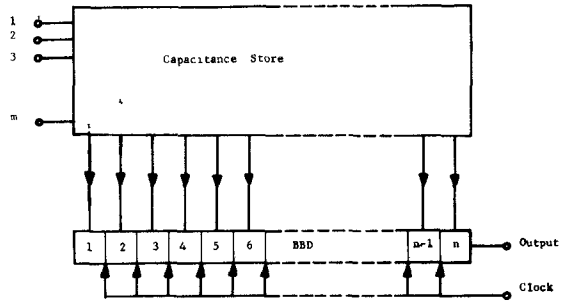

Fig. 1. Block diagram of the analog read-only memory (AROM).

The circuits consist of a BBD with 92 stages and a capacitance matrix, each row of which contains 92 capacitors. In the particular test layout the number of rows is only 3. With each capacitor in the matrix is associated a MOS transistor that establishes the connection to the BBD. Also contained in the circuit is a row of inhibit transistors and a row of clear transistors. These are only used for clearing the matrix of charge, and in the explanation of the charge transfer between matrix and BBD the inhibit transistors are assumed to be conducting while the clear transistors are nonconducting.

A. Charge Transfer from Capacitance Row to BBD

In our experiment the third row in the matrix is used for investigation of charge transfer from capacitance row to BBD.

To begin with, the capacitors C in the BBD are assumed to have zero voltage. The other capacitors C' in the BBD are charged to the voltage $U_0 - V_T$. U_0 is the amplitude of the clock pulses for the BBD and V_T is the threshold voltage of the MOS transistors.

A reference pulse of amplitude V_{ref} is applied to all capacitors $C_{3\,1}$ to $C_{3\,92}$ and a gatepulse V_{g3} is applied to the associated transistors $T_{3\,1}$ to $T_{3\,92}$. Each transistor in the third row then has $V_{ds} = V_{\text{ref}}$ and $V_{gs} = V_{g3}$. If $V_{gs} > V_T$, the transistors will conduct and a current will charge C until the source voltage V_s reaches a value V_j. V_j is the jth sample value of the analog signal. The current flow will continue until either $V_{gs} = V_T$ or $V_{ds} = 0$. $V_{gs} = V_T$ implies that $V_s = V_{g3} - V_T$, giving the same voltage on all capacitors C in the BBD, and is consequently of no interest. V_{gs} must have a value that ensures $V_{gs} > V_T$. In this case the transfer stops when $V_{ds} = 0$, and

$$V_d = V_s = V_j = \frac{C_j}{C_j + C} V_{\text{ref}} \tag{1}$$

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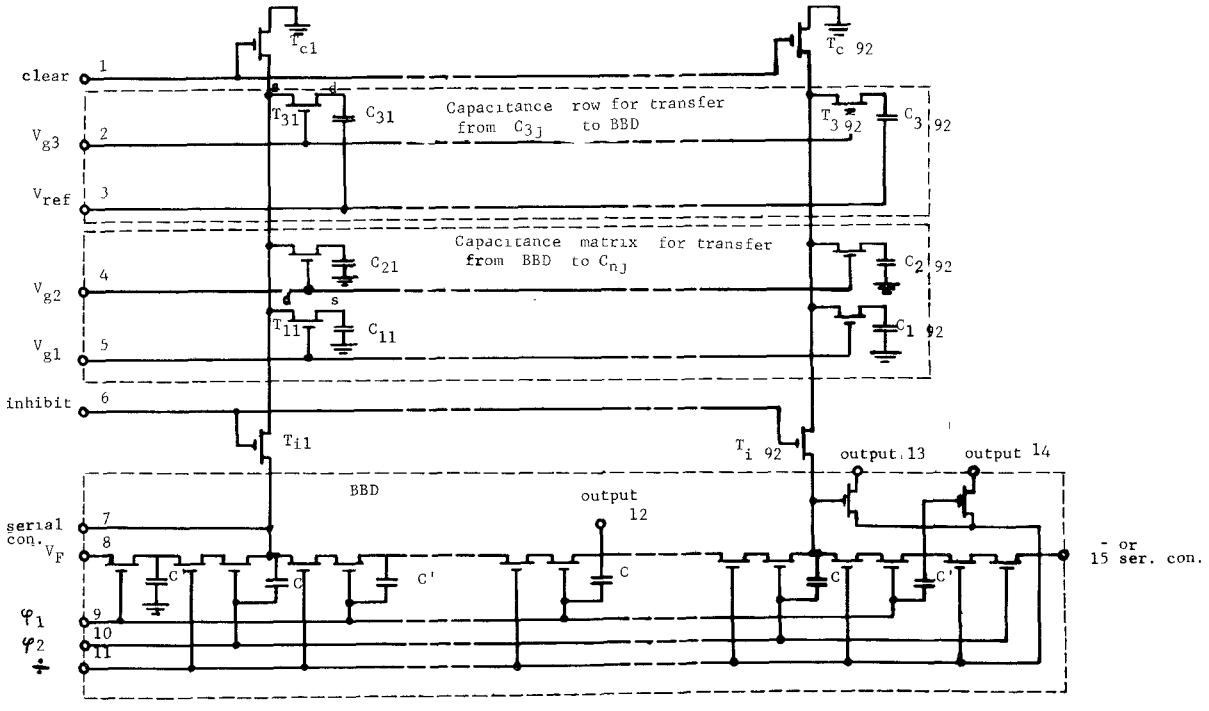


Fig. 2. Diagram of the AROM chip.

is obtained by a capacitive voltage division of V_{ref}. In order to ensure $V_{gs} > V_T$, V_{g3} must fulfill the following condition:

$$V_{g3} > \frac{C_{j\max}}{C_{j\max} + C} V_{ref} + V_T. \tag{2}$$

$C_{j\max}$ is the maximum value of C_j in the third capacitance row.

B. Charge Transfer from BBD to Capacitance Row

The two first rows in the matrix are used for investigation of charge transfer from BBD to capacitance row.

The capacitors C' in the BBD are again assumed to be charged to $U_0 - V_T$. The capacitors C are charged to a voltage V_F. This is obtained by applying V_F at the serial input (terminal 8) of the BBD. The capacitors C_{1j} and C_{2j} in the first and second row of the matrix are connected to ground.

To obtain a charge transfer from the capacitors C in the BBD to the capacitors C_{1j} in the first row of the matrix, a pulse V_g is applied to the gates of the transistors T_{1j}, and, simultaneously, a clock pulse $\phi_2 = U_0$ is applied to the capacitors C. The transistors T_{1j} obtain the initial condition $V_{ds} = U_0 + V_F$ and $V_{gs} = V_g$, and a current will flow and charge C_{1j} to a voltage V_s. Notice that in Fig. 2 source and drain of T_{1j} have been reversed compared to source and drain of T_{3j} because the direction of current flow has changed. The current flow will cease when $V_{ds} = 0$ or $V_{gs} = V_T$.

1) Capacitive Voltage Division from BBD to Capacitance Row: The first case, $V_{ds} = 0$, gives a capacitive division of the voltage $U_0 + V_F$ between C and C_j, and the result is

$$V_s = V_d = V_j = \frac{C}{C + C_j}(U_0 + V_F). \tag{3}$$

Returning V_g and ϕ_2 to ground results in

$$V_j = \frac{C}{C + C_j}(U_0 + V_F) - U_0. \tag{4}$$

The condition for obtaining capacitive voltage division is that $V_{gs} > V_T$ or

$$V_g > \frac{C}{C_{j\min} + C}(U_0 + V_F) + V_T \tag{5}$$

where $C_{j\min}$ is the minimum capacitor in the row.

2) Bucket-Brigade (BB) Transfer from BBD to Capacitance Row: The second case, $V_{gs} = V_T$, gives $V_s = V_g - V_T$. The charge on C_j then is

$$Q_j = (V_g - V_T) C_j. \tag{6}$$

As this charge has been removed from C the voltage on C will be

$$V_j = V_F + U_0 - \frac{Q_j}{C} = V_F + U_0 - (V_g - V_T)\frac{C_j}{C}. \tag{7}$$

Returning V_g and ϕ_2 to ground results in

$$V_j = V_F - (V_g - V_T)\frac{C_j}{C}. \tag{8}$$

As this transfer mechanism is the same as the one that controls the charge transport between the capacitors in a BBD during a serial transfer it is called bucket-brigade (BB) transfer.

The condition for obtaining this kind of transfer is that V_d is always greater than V_s, or

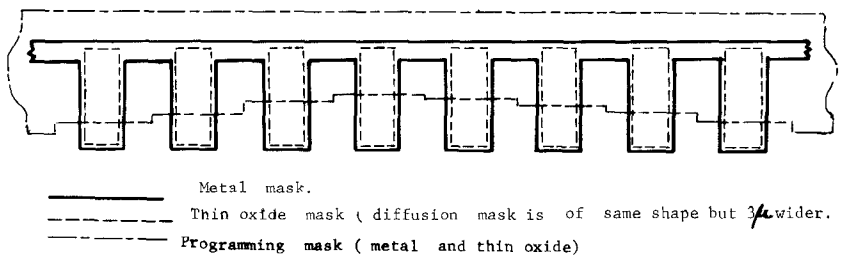


Fig. 3. Principle of mask for programming the capacitance values in the matrix.

$$V_F + U_0 - (V_g - V_T)\frac{C_j}{C} > V_g - V_T$$

$$\Rightarrow V_g < \frac{C}{C_{j\max} + C}(U_0 + V_F) + V_T. \quad (9)$$

C. Incomplete Charge Transport

The calculated values of V_j given in (1), (4), and (8) are limits obtained with infinite pulselengths. As the applied gate pulses have only a finite duration, a calculation of the dynamics of the charge transfer is necessary in order to give an estimate of the deviations from the simple expressions given above. Such a calculation has been carried out on the basis of a simple transistor model. The calculations are straightforward but rather tedious, so only the conclusion will be given here: it appears that the capacitive voltage division is approximately ten times faster than the BB transfer, but in both cases the transfer is so fast that the deviation of V_j from the values calculated from the simple expressions is less than 1 percent for pulselengths greater than 10 μs, which is the smallest clock pulselength that gives satisfactory operation of the BBD shift register. Further, it should be noticed that only differences in the deviations from the ideal sample values will be a source of signal distortion. Equal errors only give a dc level shift. Finally, it can be concluded that (1), (4), and (8) can be used without modifications for incomplete charge transfer.

D. Clearing of the Capacitance Matrix

After charge transfer, the capacitors in the matrix will contain a charge that has to be removed before the next charge transfer can take place. To remove the charge from a capacitor C_{kj} the p diffusion side of C_{kj} has to be grounded. This can only be done through the associated transistor T_{kj}. A gate pulse opens T_{kj}, and the jth column in the matrix is grounded by applying a gate pulse to the clear transistor T_{cj} (index c for clear). To prevent the capacitors C in the BBD from being discharged, a row of transistors T_{ij} (index i for inhibit) is placed between the matrix and the BBD.

III. Design Objectives

A. Layout

The BBD is implemented with tetrode transistors in order to obtain the best transport parameter α. The geometry is standard as shown in [5]. The size of the capacitors in the BBD is approximately 1.6 pF (60 μm by 80 μm). Source-follower output buffers are provided at the serial output of the BBD.

The capacitance matrix is made with the same p diffusion area for all capacitors, thus obtaining the same parasitic capacitance to substrate from all memory elements. The programming of capacitor size is done by a special mask which is used in both the thin oxide step and the aluminum step. The principle is shown in Fig. 3. Parts of the diffused areas do not have thin oxide and are not covered by aluminum. The use of a special mask for defining the capacitor values greatly facilitates reprogramming. In the test circuit, two rows (row 1 and row 2) have been programmed for BB transfer of charge from the shift register to the capacitor row. The encoded signals are a sine wave and a triangular wave, respectively. The third row has been programmed for capacitive voltage division and is encoded to generate a triangular wave. It can be used for investigating voltage division both from the capacitance row to the BBD and vice versa, since a signal sample V_j obtained in the BBD after charge transfer shows the same dependence on C_j in the two cases. This can be seen by rewriting (4):

$$V_j = V_F - \frac{C_j}{C + C_j}(U_0 + V_F). \quad (10)$$

When comparing this expression to (1) it is seen that in both cases the signal waveform is determined by $C_j/(C + C_j)$.

The maximum size of the matrix capacitors is approximately 0.85 pF (32 μm by 79 μm). The accuracy which can be obtained depends on the tracking of the various capacitors and this is inherently good because of small tolerances on masks and small variations in oxide thickness within each chip.

In the calculation of the capacitor values C_j all parasitic capacitances have been taken into consideration. The most important parasitic capacitances are the junction capacitances from the capacitors in the BBD to substrate and from the matrix capacitors to substrate. When these are taken into account, (1), (3), and (7) should be modified to

$$V_d = V_s = V_j = \frac{C_j}{C_j + C_{pj} + C + C_p} V_{\text{ref}} \quad (11)$$

$$V_j = \frac{C}{C + C_p + C_j + C_{pj}}(U_0 + V_F) \quad (12)$$

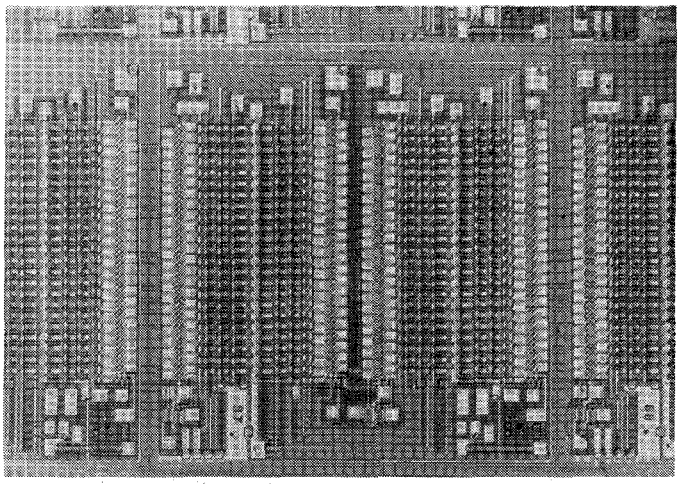
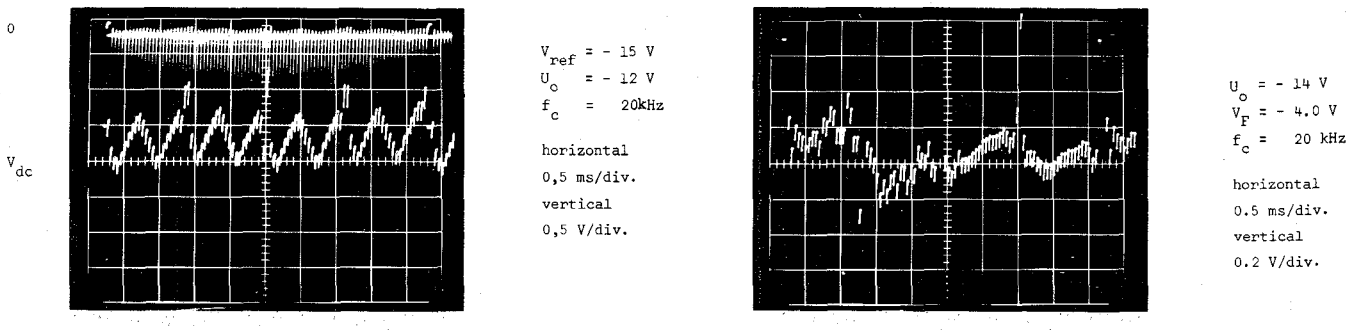


Fig. 4. AROM 3 by 3 mm^2 test chip.



(a) (b)

Fig. 5. Output signals from BBD. (a) Voltage division from capacitance matrix to BBD. (b) BB transfer from BBD to capacitance matrix.

$$V_j = V_F + U_0 - (V_g - V_T)\frac{C_j + C_{pj}}{C + C_p} \tag{13}$$

where C_p is the junction capacitance from the p diffusion side of C to substrate, and C_{pj} is the junction capacitance from the p diffusion side of C_j to substrate. For the parasitic junction capacitors, the capacitance value per square unit will be approximately 10 percent of the desired oxide capacitances.

B. Technology

The AROM is produced using standard p-channel technology. The substrate is 5-9 Ω · cm n-type ⟨100⟩. Thin oxide t_{ox} = 1000 Å. Threshold voltage V_T = 2.2 V. (Calculated value.) The AROM circuit is shown in Fig. 4.

IV. Test Results

Measurements on AROM circuits show wafer yields from 0 to 17 percent. Fig. 5 shows the triangular output signals. Voltage division gives the best result with no attenuation or DC level shift. Only an error from a noncompensated parasitic wiring capacitance is noticed. BB transfer from BBD to capacitance matrix may also give good results, but the output is dependent on the threshold voltage of transistor T_{kj} as given in (7). If V_T is not the same for all transistors in the row, noise will be imposed on the output signal as shown in Fig. 5(b).

To evaluate the output signal, peak voltages are measured from the source follower output of the BBD and divided by the source follower amplification. Fig. 6 shows the dependence of normalized peak output voltage versus clock amplitude U_0 and reference voltage V_{ref} for BB transfer and voltage division, respectively. The results show the expected linear dependence close to the theoretical values. In Fig. 6(a) an extraordinary high value of V_T gives a shift of the curve. In Fig. 6(b) a shift of the curve is also noticed. This is due to an offset in the clock voltages: instead of switching between 0 and U_0, ϕ_1 and ϕ_2 switches between V_{off} and U_0, where V_{off} is a dc offset voltage of approximately 2 V.

V. Conclusion

It can be concluded that it is possible to construct an analog memory with a capacitance matrix and a BBD readout. Capacitive voltage division is the best method for information transport from matrix to BBD unless the threshold voltages

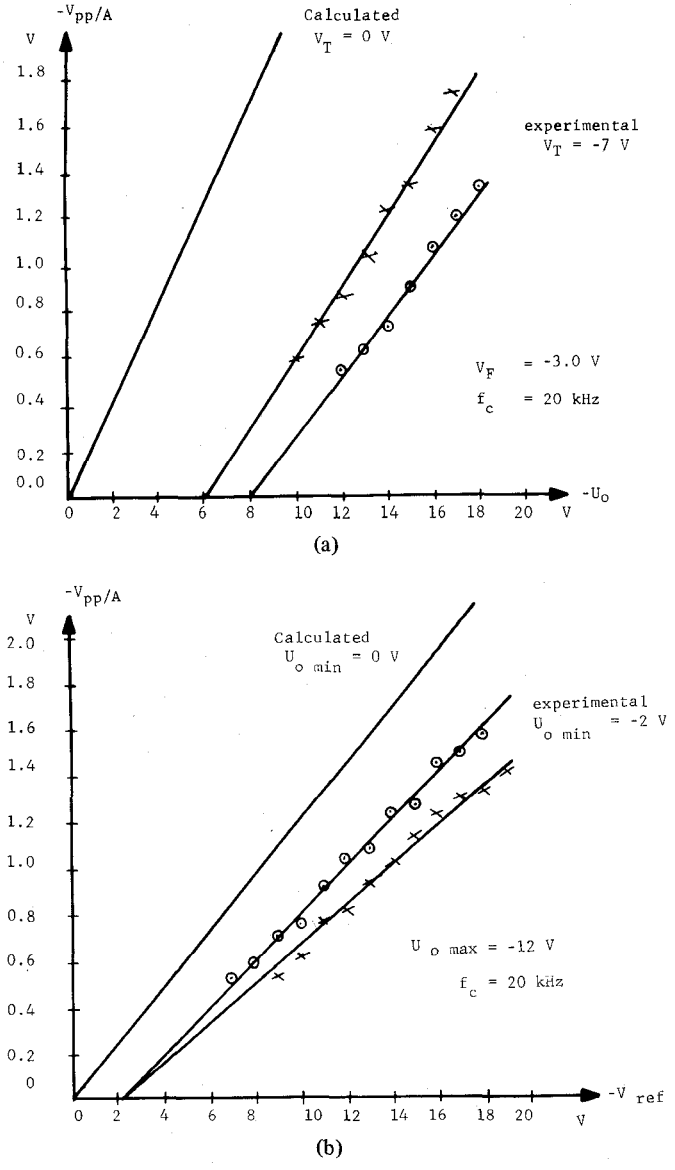


Fig. 6. Output peak voltage normalized with source follower amplification as (a) function of clock amplitude and (b) reference voltage V_{ref}.

show extremely low variation. Both theory and experiments show that charge transfer between matrix and BBD in all cases are faster than the serial transfer in the BBD. The limits in speed and clock frequency are the fundamental limits of the BBD.

If a BBD with 500 elements is required, which is the case in many applications, and standard tolerances are used the chip size will be 3 by 10 mm for only three rows. Thus if larger memory systems are needed hybrid solutions may be used.

Acknowledgment

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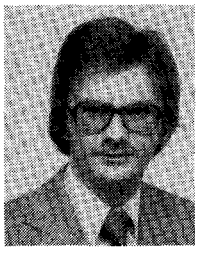

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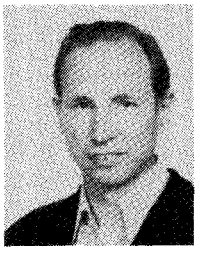

Ole Olesen was born in Fyen, Denmark, on February 16, 1932. He received the M.S. degree in electrical engineering and the Lic. Techn. degree (comparable to the Ph.D. degree) from the Technical University of Denmark, Lyngby, in 1958 and 1970, respectively.

From 1958 to 1960 he worked in the electronic department of the Royal Danish Airforce on problems concerning airborne navigation equipment. From 1960 to 1967 he was a member of the Research and Teaching Staff of the Electronics Laboratory and from 1967 at the Laboratory for Semiconductor Devices both at the Technical University of Denmark. He is now Associate Professor. His research interests are in the area of charge transfer devices and semiconductor memories.

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